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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,793	09/30/2003	Lowell Raymond Pearl	P16625	2241

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EXAMINER	
YANCHUS III, PAUL B	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,793	PEARL, LOWELL RAYMOND	
	Examiner	Art Unit	
	Paul B. Yanchus	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 11 and 12 are rejected under 35 U.S.C. 102(b) as being anticiapted by Hwang, US Patent no. 5,714,873.

Regarding claim 11, Hwang discloses an apparatus, comprising:

a detector circuit to detect a processor type [column 9, lines 23-37 and Figure 6]; and

a voltage provider circuit to provide a processor voltage in accordance with the processor type [column 9, lines 35-52 and Figure 6].

Regarding claim 12, Hwang discloses that the voltage provider circuit provides a first voltage level when a first processor type is detected and a second voltage level when a second processor type is detected [column 9, lines 35-52].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9, 10, 13-20 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang, US Patent no. 5,714,873, in view of Menezes et al., US Patent no. 6,845,456 [Menezes].

Regarding claim 1, Hwang discloses an apparatus, comprising:

a detector circuit to detect a processor type [column 9, lines 23-37 and Figure 6]; and

a voltage provider circuit to provide a processor voltage in accordance with the processor type [column 9, lines 35-52 and Figure 6].

Hwang discloses detecting a processor type and providing an operating voltage to the processor based on the detected processor type, but does not disclose providing a low-power state voltage to the processor. Menezes discloses detecting a processor type and providing a low-power state voltage to the processor based on the processor type to ensure that the proper operating voltage is supplied to the processor in all power modes [column 10, line 42 – column 11, line 5]. It would have been obvious to one of ordinary skill in the art to modify the Hwang apparatus to provide a low-power state voltage to the processor in addition to a normal high-power state voltage in order to ensure that the proper operating voltage is supplied to the processor in all power modes.

Regarding claim 2, Hwang further discloses that the detector detects the processor type in accordance with a signal from a processor pin [column 9, lines 35-52 and Figure 6].

Regarding claims 3 and 4, Hwang discloses a switching element [SW325], which is either in an on state or an off state depending on the type of processor [column 9, lines 35-52 and Figure 6]. Hwang is silent as to how the switch is implemented. Bi-polar junction transistor switches are well known in the art and it would have been obvious to one of ordinary skill in the

art to use a well known bi-polar junction transistor switch as the switching element in the Hwang apparatus.

Regarding claim 5, Hwang discloses that the voltage provider circuit provides a first voltage level when a first processor type is detected and a second voltage level when a second processor type is detected [column 9, lines 35-52].

Regarding claim 6, Hwang discloses that the voltage provider comprises a voltage divider [Figure 6].

Regarding claims 7 and 8, Hwang discloses a switching element [SW325], which adjusts a resistance depending on the type of processor [column 9, lines 35-52 and Figure 6]. Hwang is silent as to how the switch is implemented. Transistor switches are well known in the art and it would have been obvious to one of ordinary skill in the art to use a well known transistor switch as the switching element in the Hwang apparatus.

Regarding claim 10, Hwang further discloses that the detector circuit and the voltage provider circuit are associated with a voltage regulator integrated circuit [column 9, lines 18-22 and Figure 6].

Regarding claim 13, Hwang discloses an apparatus, comprising:

an input to receive a signal associated with a processor type [column 9, lines 23-37 and Figure 6]; and

an output to provide a processor voltage in accordance with the processor type [column 9, lines 35-52 and Figure 6].

Hwang discloses detecting a processor type and providing an operating voltage to the processor based on the detected processor type, but does not disclose providing a low-power

state voltage to the processor. Menezes discloses detecting a processor type and providing a low-power state voltage to the processor based on the processor type to ensure that the proper operating voltage is supplied to the processor in all power modes [column 10, line 42 – column 11, line 5]. It would have been obvious to one of ordinary skill in the art to modify the Hwang apparatus to provide a low-power state voltage to the processor in addition to a normal high-power state voltage in order to ensure that the proper operating voltage is supplied to the processor in all power modes.

Regarding claim 14, Hwang discloses that the voltage provider circuit provides a first voltage level when a first processor type is detected and a second voltage level when a second processor type is detected [column 9, lines 35-52].

Regarding claim 15, Hwang further discloses that the input receives a signal from a processor pin [column 9, lines 35-52 and Figure 6].

Regarding claim 16, Hwang further discloses that the output provides an output voltage to a processor pin [Figure 6].

Regarding claim 17, Hwang discloses a switching element [SW325], which adjusts a resistance to control an output voltage depending on the type of processor [column 9, lines 35-52 and Figure 6]. Hwang is silent as to how the switch is implemented. Transistor switches are well known in the art and it would have been obvious to one of ordinary skill in the art to use a well known transistor switch as the switching element in the Hwang apparatus.

Hwang does not disclose providing a low-power state voltage to the processor. Menezes discloses detecting a processor type and providing a low-power state voltage to the processor based on the processor type to ensure that the proper operating voltage is supplied to the

processor in all power modes [column 10, line 42 – column 11, line 5]. It would have been obvious to one of ordinary skill in the art to modify the Hwang apparatus to provide a low-power state voltage to the processor in addition to a normal high-power state voltage in order to ensure that the proper operating voltage is supplied to the processor in all power modes.

Regarding claim 18, Hwang further discloses that the apparatus comprises a voltage regulator integrated circuit [column 9, lines 18-22 and Figure 6].

Regarding claim 19, Hwang discloses a method comprising:

detecting a processor type [column 9, lines 23-37 and Figure 6]; and

providing a processor voltage in accordance with the processor type [column 9, lines 35-52 and Figure 6].

Hwang discloses detecting a processor type and providing an operating voltage to the processor based on the detected processor type, but does not disclose providing a low-power state voltage to the processor. Menezes discloses detecting a processor type and providing a low-power state voltage to the processor based on the processor type to ensure that the proper operating voltage is supplied to the processor in all power modes [column 10, line 42 – column 11, line 5]. It would have been obvious to one of ordinary skill in the art to modify the Hwang apparatus to provide a low-power state voltage to the processor in addition to a normal high-power state voltage in order to ensure that the proper operating voltage is supplied to the processor in all power modes.

Regarding claim 20, Hwang discloses providing a first voltage level when a first processor type is detected and a second voltage level when a second processor type is detected [column 9, lines 35-52].

Regarding claim 22, Hwang discloses a system comprising:

a power supply to convert alternating current power to direct current power [inherent that the power supply has an AC/DC converting means]; and

a voltage regulator coupled to the power supply and including:

a detector circuit to detect a processor type [column 9, lines 23-37 and Figure 6], and

a voltage provider circuit to provide a processor voltage in accordance with the processor type [column 9, lines 35-52 and Figure 6].

Hwang discloses detecting a processor type and providing an operating voltage to the processor based on the detected processor type, but does not disclose providing a low-power state voltage to the processor. Menezes discloses detecting a processor type and providing a low-power state voltage to the processor based on the processor type to ensure that the proper operating voltage is supplied to the processor in all power modes [column 10, line 42 – column 11, line 5]. It would have been obvious to one of ordinary skill in the art to modify the Hwang apparatus to provide a low-power state voltage to the processor in addition to a normal high-power state voltage in order to ensure that the proper operating voltage is supplied to the processor in all power modes.

Regarding claim 23, Hwang discloses providing a first voltage level when a first processor type is detected and a second voltage level when a second processor type is detected [column 9, lines 35-52].

Claims 9 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang, US Patent no. 5,714,873 and Menezes et al., US Patent no. 6,845,456 [Menezes], in view of Gebara et al., US Patent no. 6,035,407 [Gebara].

Hwang and Menezes, as desbribed above, disclose detecting a processor type and providing low-power state operating voltage to the processor based on the detected processor type, but do not disclose an offset voltage circuit to adjust an offset value associated with a processor voltage in accordance with the processor type. However, using offset values to adjust a supply voltage is well known in the art. Gebara discloses using an offset value to adjust the voltage supplied to a processor [column 8, lines 10-30]. It would have been obvious to one of ordinary skill in the art to use well known offset values to adjust the voltage supplied to the processor in the Hwang and Menezes apparatus.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Vyssotski et al., US Patent Application Publication no. 2004/0019815, discloses selecting a proper voltage to be supplied to a load with multiple operating states.

Yu et al., US Patent no. 6,944,783, discloses identifying a processor and supplying power to the processor depending on the processor type.

Isaac et al., US Patent no. 6,327,663, discloses detecting signals from one more pins of a processor and supplying power to the processor based on the signals.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B. Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus
March 18, 2006